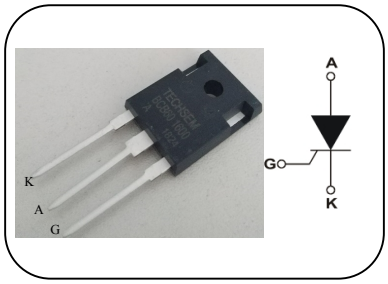


Features：

Planar passivated chip
Long-term stability

Typical Applications：

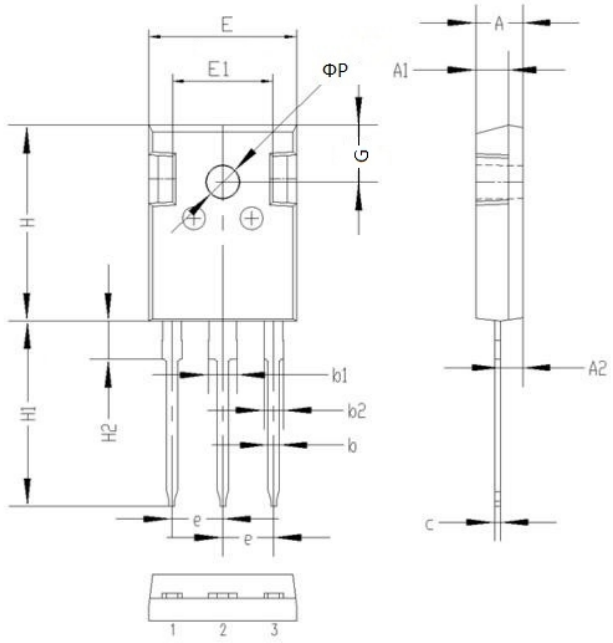
Softstart AC motor control
DC Motor control
Power converter
AC power control

$I_{T(RMS)}$ **60A**
V_{DRM}/V_{RRM} **1600V**
I_{GT} **20mA~100mA**

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(RMS)}$	RMS on-state current	180 half sine wave 50Hz T_C=70°C	125			60	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	tp=10ms	25			1600	V
I_{DRM} I_{RRM}	Repetitive peak off-state current Repetitive peak reverse current	at V_{DRM}/V_{RRM}	25			100	μA
			125			10	mA
I_{TSM}	Surge on-state current	10ms half sine wave	25			600	A
I^2t	I^2t value for fusing					1800	A^2s
V_{TM}	Peak on-state voltage	I_{TM}=60A, tp=380μs	25			1.60	V
di/dt	Critical rate of rise of on-state current	I_G=2*I_{GT}	25			100	A/μs
dv/dt	Critical rate of rise of off-state voltage	V_D=2/3V_{DRM}, Gate Open	125			700	V/μs
I_{GT}	Gate trigger current	V_D=12V R_L=33Ω	25	20		100	mA
V_{GT}	Gate trigger voltage					1.5	V
I_H	Holding current	I_T=500mA	25	10		150	mA
I_L	Latching current	I_G=1.2 I_{GT}	25			250	mA
V_{GD}	Non-trigger gate voltage	V_D=V_{DRM} R_L=3.3kΩ	125			0.2	V
I_{GM}	Peak gate current					5	A
$P_{G(AV)}$	Average gate power dissipation					1	W
P_{GM}	Peak gate power					10	W
$R_{th(j-c)}$	Thermal resistance Junction to case				0.8		C /W
T_{stg}	Storage junction temperature range			-40		150	C
T_j	Operating junction temperature			-40		125	C
Outline	TO-247						

Outline:

TO-247 PACKAGE



Symbol	Dimensions(millimeters)	
	Min.	Max.
A	4.80	5.20
A1	3.30	3.70
A2	2.10	2.50
b	1.00	1.40
b1	2.90	3.30
b2	1.90	2.30
c	0.40	0.80
e	5.25	5.65
E	15.6	16.0
E1	10.6	11.00
H	20.8	21.2
H1	19.4	20.4
H2	3.90	4.30
G	5.90	6.30
ΦP	3.30	3.70